What is claimed is:

1. Apparatus for the design of logic circuits, comprising:
    a. a computer, and
    b. software stored on the computer for
        b1. representing multilevel logic schema in vector form; and for
        b2. simplifying multilevel logic schema into a simplified form by exploiting symmetries in the logical schema.

2. The apparatus of claim 1 in which simplifying multilevel logic schema comprises eliminating opposing couples.

3. A method of reducing multilevel logic to simpler form comprising the steps of:
    a. representing the logic in vector form; and
    b. removing redundancy by eliminating opposing couples.

4. The method of claim 3 further comprising the step of:
    c. sliding symmetrical portions of the logic attached to opposing couples onto a point common to the opposing couples.

5. A system for the design or manufacturing of logical circuits, comprising:
    a. a plurality of computers connected to a network;
    b. at least one of said computers having software stored thereof for
        b1. representing multilevel logic schema in vector form; and for
        b2. simplifying multilevel logic schema into a simplified form by exploiting symmetries in a logical schema.

6. The system of claim 5 in which a computer having said software communicates logical schema to one or more other computing devices.

7. The system of claim 5 in which the software eliminates opposing couples in simplifying multilevel logic.

8. A computer program product, comprising:
    a. a computer readable storage medium; and
    b. at least one computer program stored on said storage medium, said at least one computer program comprising instructions for:
        b1. representing multilevel logic schema in vector form; and for
        b2. simplifying multilevel logic schema into a simplified form by exploiting symmetries in the logical schema.

9. A computer program product, comprising:
    a. a computer readable storage medium; and
    b. at least one computer program stored on said storage medium, said at least one computer program comprising instructions for:

b1. representing the logic in vector form; and
b2. removing redundancy by eliminating opposing couples.

10. A method of manufacturing integrated circuits comprising the steps of:
a. representing at least a portion of the logic circuits to be incorporated into the integrated circuit in vector form; and
b. simplifying the logic by removing redundancy by eliminating opposing couples.

11. A method of manufacturing integrated circuits comprising the steps of:
a. representing at least a portion of the logic circuits to be incorporated into the integrated circuit in vector form; and
b. simplifying the logic by removing redundancy by exploiting symmetries in the logical schema.

12. A method of reducing multilevel logic to simpler form comprising the steps of:
a. representing the logic in vector form;
b. identifying opposing couples having at least symmetrical logic comprising some similarities in logical expression that connects to them;
c. removing redundancy by eliminating an opposing couples and sliding the symmetrical logic attached to opposing couples onto a point common to the opposing couples.